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(57) Abstract :
 The present invention discloses a customizable device (100) for emulating multicore architectures in real time. It comprises programmable logic cores (102), configurable cache modules (104), reprogrammable bus interconnects (106), and memory blocks (108). A graphical interface (110) allows dynamic adjustment of core count, topology, and memory configurations. Integrated monitoring circuits (112) and debugging ports (116) enable real-time performance and thermal analysis, making the device ideal for research, development, and education in processor architecture and parallel computing environments.

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